CLAIMS

What is claimed is:

1. An SRAM comprising:

first and second access NMOS transistors;

a first drive NMOS transistor and a first load PMOS transistor which constitute a first inverter which is selectively activated in response to the operation of the second access NMOS transistor; and

a second drive NMOS transistor and a second load PMOS transistor which constitute a second inverter which is selectively activated in response to the operation of the first access NMOS transistor,

wherein the transistors are formed on active areas of an SOI substrate, and wherein a portion of an active area where a load PMOS transistor is formed extends so as to make a predetermined angle with a portion of an active area where a drive NMOS transistor is formed.

2. The SRAM of claim 1, wherein the predetermined angle is between 30° and 60° .

3. The SRAM of claim 1, wherein the predetermined angle is 45° .

4. The SRAM of claim 1, wherein the portion of the active area where a load PMOS transistor is formed extends in a [110] silicon crystallization growth direction.

5. The SRAM of claim 1, wherein the active area comprises:

a first active area where the first access NMOS transistor and the first inverter are formed; and

a second active area where the second access NMOS transistor and the second inverter are formed.

6. The SRAM of claim 5, wherein the drain region of the first drive NMOS transistor and the drain region of the first load PMOS transistor contact each other on the first active area of a silicon layer of the SOI substrate, and wherein the drain region of the second drive NMOS transistor and the drain region of the second load PMOS transistor contact each other on the second active area of the silicon layer of the SOI substrate.

7. The SRAM of claim 6, wherein one of the drain and source of the first access NMOS transistor, the drain of the first drive NMOS transistor, and the drain of the first load PMOS transistor are formed in a shared region of the first active area so as to be electrically connected to one another, and wherein one of the drain and source of the second access NMOS transistor, the drain of the second drive NMOS transistor, and the drain of the second load PMOS transistor are formed in a shared region of the second active area so as to be electrically connected to one another.

8. The SRAM of claim 1, wherein one of the drain and source of the first access NMOS transistor, the drain of the first drive NMOS transistor, and the drain of the first load PMOS transistor are formed in a shared region of the first active area so as to be electrically connected to one another, and wherein one of the drain and source of the second access NMOS transistor, the drain of the second drive NMOS transistor, and the drain of the second load PMOS transistor are formed in a shared region of the second active area so as to be electrically connected to one another.

9. An SRAM comprising:

a semiconductor substrate;

a first active area formed on the semiconductor substrate and having a first access NMOS transistor and a first inverter which is comprised of a first drive NMOS transistor and a first load PMOS transistor; and

a second active area formed on the semiconductor substrate and having a second access NMOS transistor and a second inverter which is comprised of a second drive NMOS transistor and a second load PMOS transistor,

wherein a portion of each of the first and second active areas where the first and second load PMOS transistors are formed, respectively, extends so as to make a predetermined angle with a portion of each of the first and second active areas where the NMOS transistors are formed.

10. The SRAM of claim 9, wherein the predetermined angle is between 30° and 60° .

11. The SRAM of claim 9, wherein the predetermined angle is 45° .

12. The SRAM of claim 9, wherein the portion of the active area where a load PMOS transistor is formed extends in the [110] silicon crystallization growth direction.

13. The SRAM of claim 9, wherein the drain region of the first drive NMOS transistor and the drain region of the first load PMOS transistor contact each other on the first active area of the semiconductor substrate, and wherein the drain region of the second drive NMOS transistor and the drain region of the second load PMOS transistor contact each other on the second active area of the semiconductor substrate.

14. The SRAM of claim 13, wherein one of the drain and source of the first access NMOS transistor, the drain of the first drive NMOS transistor, and the drain of the first load PMOS transistor are formed in a shared region of the first active area so as to be electrically connected to one another, and wherein one of the drain and source of the second access NMOS transistor, the drain of the second drive NMOS transistor, and the drain of the second load PMOS transistor are formed in a shared region of the second active area so as to be electrically connected to one another.

15. The SRAM of claim 9, wherein one of the drain and source of the first access NMOS transistor, the drain of the first drive NMOS transistor, and the drain of the first load PMOS transistor are formed in a shared region of the first active area so as to be electrically connected to one another, and wherein one of the drain and source of

the second access NMOS transistor, the drain of the second drive NMOS transistor, and the drain of the second load PMOS transistor are formed in a shared region of the second active area so as to be electrically connected to one another.

16. The SRAM of claim 14, wherein the semiconductor substrate is an SOI substrate.

17. An SRAM formed with first and second access NMOS transistors, a first drive NMOS transistor and a first load PMOS transistor which constitute a first inverter that is selectively activated in response to the operation of the second access NMOS transistor, and a second drive NMOS transistor and a second load PMOS transistor which constitute a second inverter that is selectively activated in response to the operation of the first access NMOS transistor, the SRAM comprising:

an SOI substrate;

a first active area formed on the SOI substrate and having a first access NMOS transistor and a first inverter which is comprised of a first drive NMOS transistor and a first load PMOS transistor; and

a second active area formed on the SOI substrate and having a second access NMOS transistor and a second inverter which is comprised of a second drive NMOS transistor and a second load PMOS transistor,

wherein a portion of each of the first and second active areas where the first and second load PMOS transistors are formed, respectively, extends so as to make a predetermined angle with a portion of each of the first and second active areas where the NMOS transistors are formed.

18. The SRAM of claim 17, wherein the predetermined angle is between 30° and 60° .

19. The SRAM of claim 17, wherein the predetermined angle is 45° .

20. The SRAM of claim 17, wherein the portion of the active area where a load PMOS transistor is formed extends in the [110] silicon crystallization growth direction.

21. An SRAM formed with first and second access NMOS transistors, a first drive NMOS transistor and a first load PMOS transistor which constitute a first inverter that is selectively activated in response to the operation of the second access NMOS transistor, and a second drive NMOS transistor and a second load PMOS transistor which constitute a second inverter that is selectively activated in response to the operation of the first access NMOS transistor, the SRAM comprising:

an SOI substrate;

a first active area formed on the SOI substrate and having a first access NMOS transistor and a first inverter which is comprised of a first drive NMOS transistor and a first load PMOS transistor; and

a second active area formed on the SOI substrate and having a second access NMOS transistor and a second inverter which is comprised of a second drive NMOS transistor and a second load PMOS transistor,

wherein a portion of each of the first and second active areas where the first and second load PMOS transistors are formed, respectively, extends so as to make a predetermined angle with a portion of each of the first and second active areas where the NMOS transistors are formed,

wherein one of the drain and source of the first access NMOS transistor, the drain of the first drive NMOS transistor, and the drain of the first load PMOS transistor are formed in a shared region of the first active area so as to be electrically connected to one another, and

wherein one of the drain and source of the second access NMOS transistor, the drain of the second drive NMOS transistor, and the drain of the second load PMOS transistor are formed in a shared region of the second active area so as to be electrically connected to one another.

22. The SRAM of claim 21, wherein the predetermined angle is between 30° and 60° .

23. An SRAM formed with first and second access NMOS transistors, a first drive NMOS transistor and a first load PMOS transistor which constitute a first inverter that is selectively activated in response to the operation of the second access NMOS transistor, and a second drive NMOS transistor and a second load PMOS transistor which constitute a second inverter that is selectively activated in response to the operation of the first access NMOS transistor, the SRAM comprising:

an SOI substrate;

a first active area formed on the SOI substrate and having a first access NMOS transistor and a first inverter which is comprised of a first drive NMOS transistor and a first load PMOS transistor; and

a second active area formed on the SOI substrate and having a second access NMOS transistor and a second inverter which is comprised of a second drive NMOS transistor and a second load PMOS transistor,

wherein a portion of each of the first and second active areas where the first and second load PMOS transistors are formed extends so as to make an angle of approximately 45 degrees with a portion of each of the first and second active areas where the NMOS transistors are formed,

wherein one of the drain and source of the first access NMOS transistor, the drain of the first drive NMOS transistor, and the drain of the first load PMOS transistor are formed in a shared region of the first active area so as to be electrically connected to one another, and

wherein one of the drain and source of the second access NMOS transistor, the drain of the second drive NMOS transistor, and the drain of the second load PMOS transistor are formed in a shared region of the second active area so as to be electrically connected to one another.